Low-Cost Sample/Hold Includes Two ICs

Properly connected, a quad-SPDT analog switch and op amp (**Figure 1**) form a sample/hold circuit. The circuit enconomizes during operation by switching the op amp from input to output, thereby buffering the input (V_{IN}) during sample mode and buffering the hold capacitor (C_H) during hold mode.

The two digital inputs are compatible with TTL and CMOS logic levels. Input command $\overline{S}/H$ controls the circuit's operating mode (low is sample), and DISCH is an optional control input whose low state commands a rapid and complete discharge of C_H. Figure 2 provides a simplified functional diagram of the circuit.

A general-purpose op amp is suitable for IC_1, provided the input bias current is acceptable (bias current usually dominates the hold-mode droop rate). C_H can range from 100pF to 0.1µF. In driving such a capacitive load, most op amps will oscillate without an isolating resistor (R_1) of 100 to 200Ω within the feedback loop. Using components as shown in **Figure 1**, the typical circuit performance includes: droop rate ≤ 100mV/sec, aperture time ≤ 100nsec, offset voltage ≤ 5mV, output charge injection ≤ 25pC, and acquisition time ≤ 1µsec (for ±10% accuracy) or ≤5µsec (for ±0.1% accuracy).

Performance is about the same for ±15V or ±12V supplies, and the system also works well on a unipolar supply of 10 to 30V. Whatever the supply configuration, the op amp's common-mode range restricts V_{IN} to about 2V less than the supply rails. The control inputs' TTL/CMOS switching thresholds (0.8V max, 2.4V min) remain constant regardless of supply levels.

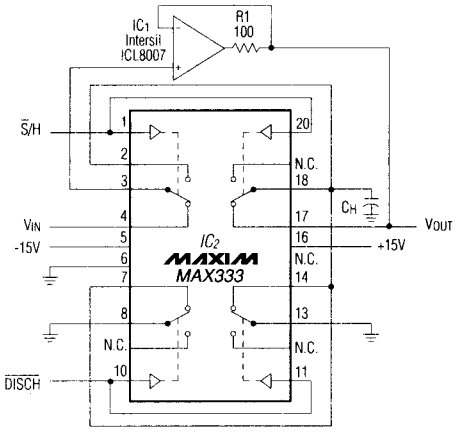

Figure 1. This quad-SPDT analog switch and general-purpose op amp form a low-cost sample/hold suitable for moderate-speed applications.

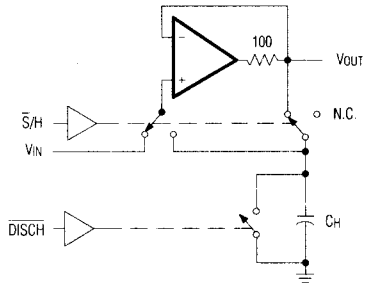

Figure 2. A simplified version of Figure 1 illustrates how the analog switches shift the op amp from the role of input buffer to that of an output hold-capacitor buffer.

(Circle 6)